Theoretical maximum NPR of a 16-bit ADC (ADI AD9467). A. Farson VA7OJ/AB4OJ

Ref. 1, Figure 2 gives the theoretical maximum NPR value of 85.4 dB for a 16-bit ADC. This value can be derived at the optimum noise loading point for $B_{RF} = f_s/2$, where $B_{RF}$ is the noise bandwidth, $f_s$ is the sampling frequency of the ADC, and assuming a perfect, noiseless ADC whose noise floor $N_0$ is:

$$N_0 = (6 \times \text{no. of bits}) + 1.76 = (6 \times 16) + 1.76 = 97.8 \text{ dBFS} \quad (1)$$

The noise floor of the ADI AD9467 ADC at 140 MHz is 75.0 dBFS, which is 22.8 dB worse than the theoretical maximum value. This assumes that the NPR test will be performed at $B_{RF} = f_s/2 = 123$ MHz. ($f_s = 246$ MHz for our example.) For the bandstop filter, $f_0 = 5340$ kHz, and $B = 3$ kHz (notch bottom).

Theoretical NPR for ADI AD9467 at 123 MHz = $85.4 - 22.8 = 62.6$ dB \hspace{1cm} (2)

Let us now derive the process gain $G_p$ due to the presence of the band-limiting filter used in the NPR test, assuming a 5.6 MHz band-limiting filter ($B_{RF} = 5.537$ MHz). Here, $f_s = 246$ MHz:

$$G_p = 10 \log_{10}(f_s / 2 * B_{RF}) = 10 \log_{10}(246 / 2 * 5.537) = 13.5 \text{ dB} \quad (3)$$

We can now predict theoretical NPR for a direct-sampling receiver incorporating the AD9467 (assuming preselector and preamp out):

$$\text{NPR} = (\text{NPR for } B_{RF} = f_s/2) + G_p = 62.6 + 13.5 = 76.1 \text{ dB} \quad (4)$$

This value is theoretical, as it assumes 0 dB insertion loss in the RF circuits ahead of the ADC input, and also that the noise loading does not provoke IMD. Practical measurements will show how close the actual implementation is to the theoretical value.